

Informal Workshop

**“Galileo Galilei (GG) and GGG lab prototype:
state of the art and new possibilities”**

10-12 February 2010, Pisa and San Piero a Grado

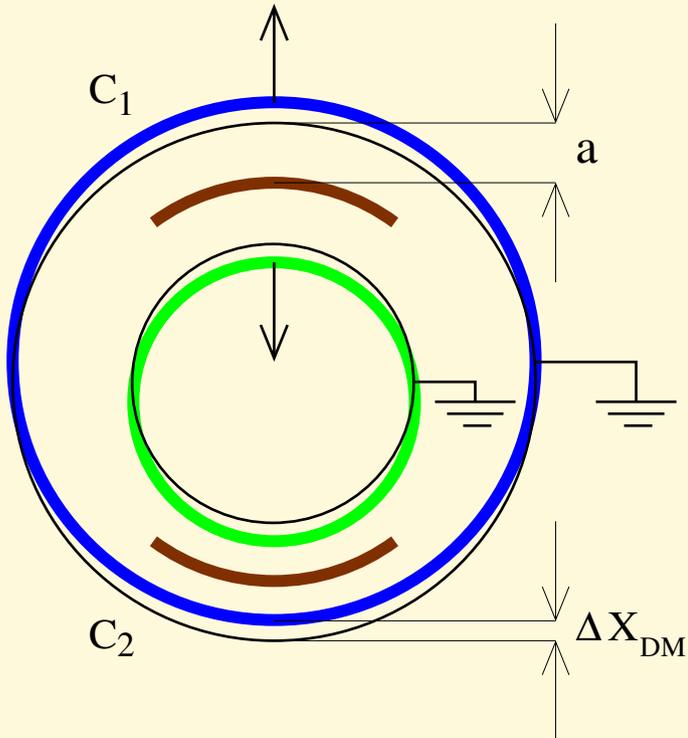
Capacitance sensing electronics: state of the art
worldwide, current status in GGG and prospects for
improvement

Raffaello Pegna, INFN Pisa.

OUTLINE

- GGG (and GG) capacitive displacement sensor.
- The noise level of the GGG capacitance bridge
- The noise level of ONERA capacitance bridge.
- The noise level of the new GGG Capacitance bridge under developement.

The two capacitance sensor of the bridge of GGG.



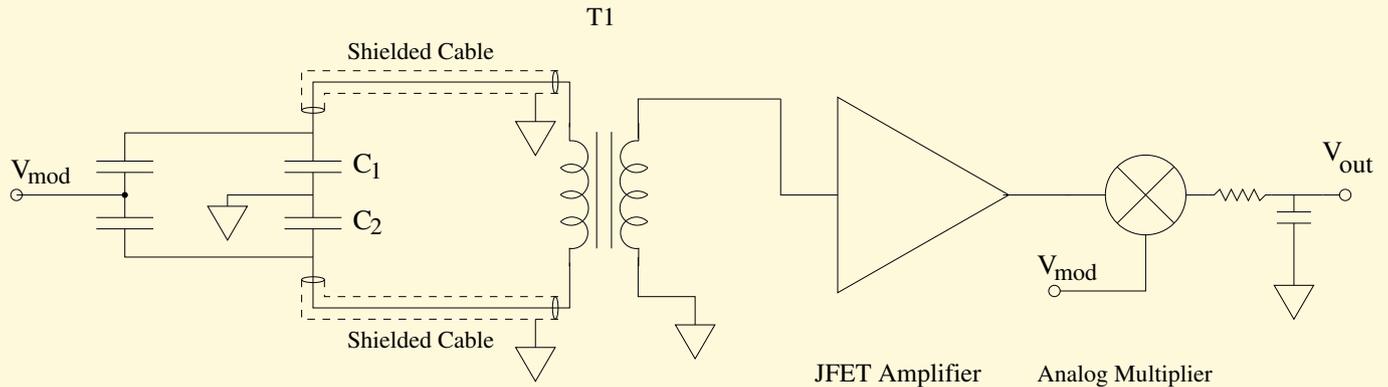
$$\frac{\Delta C}{2C_0} \simeq \frac{\Delta X_{DM}}{a}$$

In GGG: $C_0 \simeq 100$ pF and $a \simeq 1$ mm

With $\Delta C_n \simeq 10^{-7}$ pF/ $\sqrt{(\text{Hz})}$

$\Delta X_{DM} \simeq 0.5 \cdot 10^{-12}$ m/ $\sqrt{(\text{Hz})}$

Simplified schematics of the GGG bridge

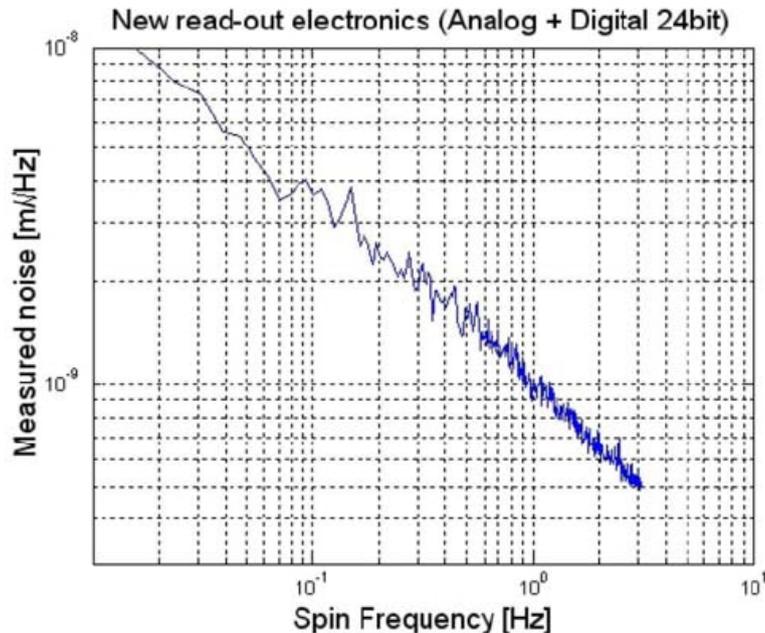


- The transformer acts as a balanced to unbalanced converter.
- The JFET amplifier is a voltage amplifier.
- The lock-in amplifier is based on an analog multiplier IC.

Measured noise of the GGG bridge.

$\sim 10^{-4} pF / \sqrt{Hz}$ at ~ 0.17 Hz, it does not limit the performance of GGG.

Advantage of high frequency modulation



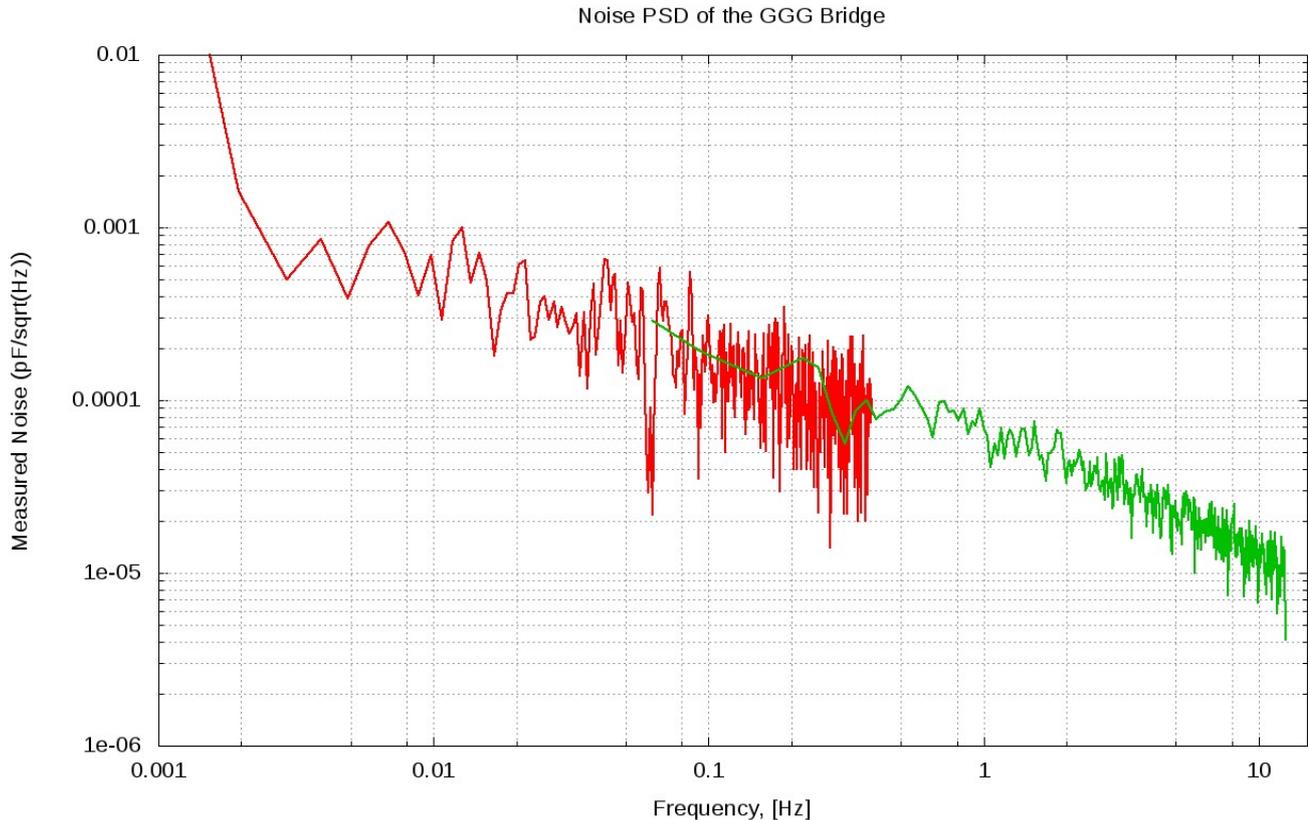
Relative displacements of GG/GGG test cylinders are read by 2 co-rotating capacitance bridges. In GGG the analog output of each bridge is digitized 32 times per turn. Plot shows, as function of spin frequency, noise of read-out electronics alone located inside a chamber at $35 \pm 0.1^\circ\text{C}$. The noise of digital part was measured for several days, sampling at 32 times per spin period (up to 3 Hz). The noise of the analog part was measured with the spectrum analyzer. Curve shows the sum of the two (2007).

Advantage of fast spin in a space test of the equivalence principle is apparent!

Measured noise of the GGG bridge.

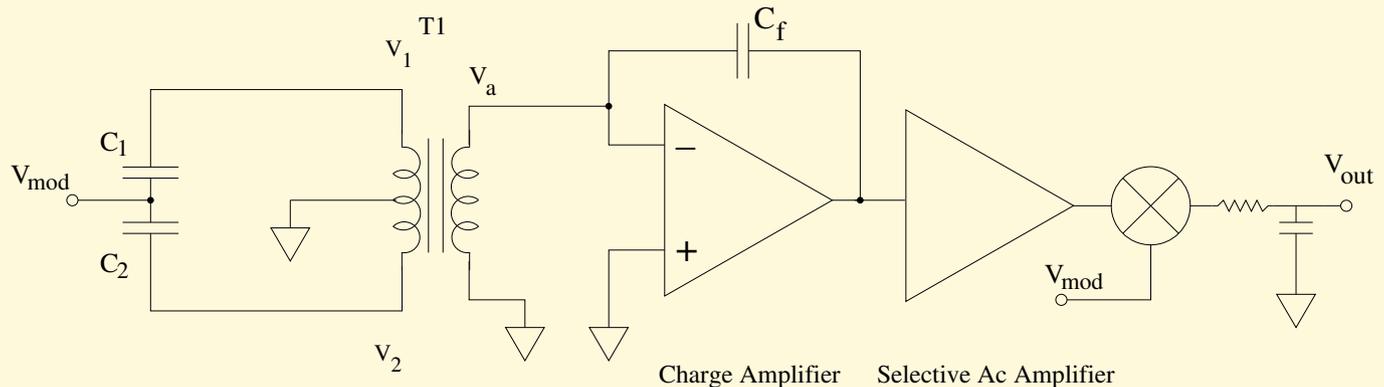
Modified version, the performance is the same.

$\sim 10^{-4} \text{pF}/\sqrt{\text{Hz}}$ at $\sim 0.17 \text{ Hz}$, it does not limit the performance of GGG.



Simplified schematics of the ONERA bridge

V. Josselin et al. Sensors and Actuators **78** (1999) 92–98.



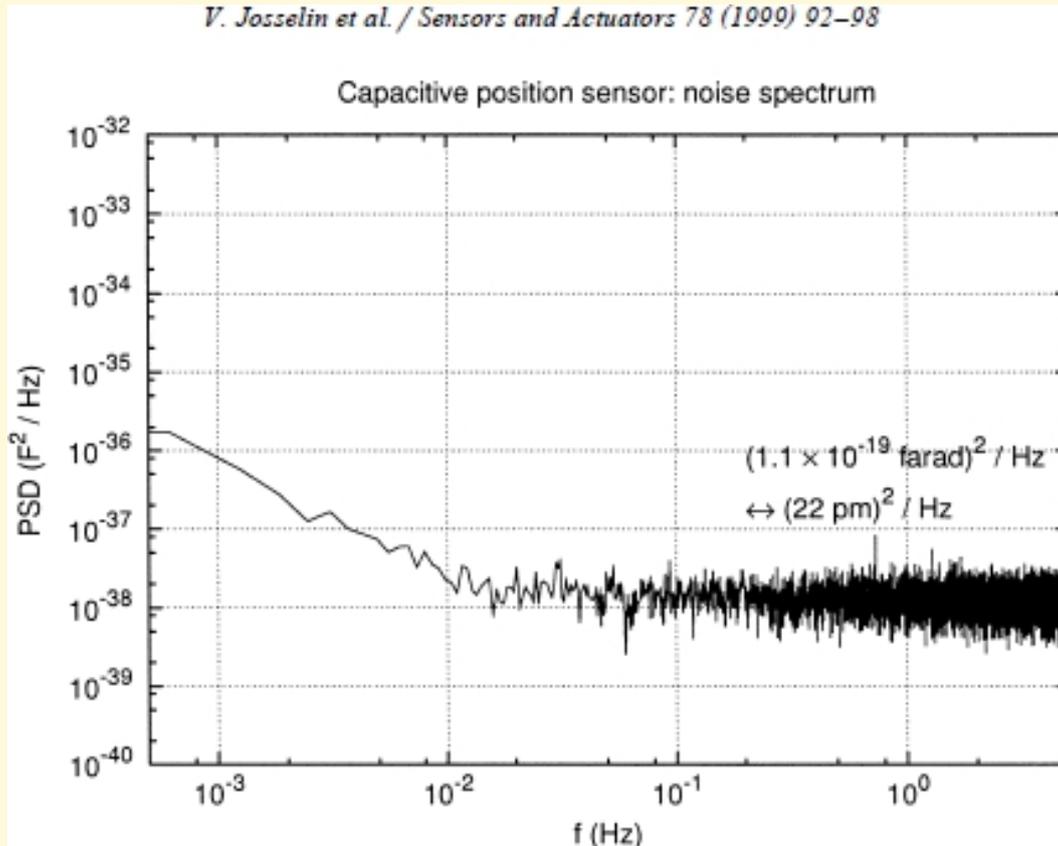
- The test mass is connected to the modulating signal.
- The primary of the transformer is connected to ground.
- The transformer is part of the bridge.
- The charge amplifier is a current amplifier.

Published noise of the ONERA bridge.

V. Josselin et al. *Sensors and Actuators* **78** (1999) 92–98.

$\sim 10^{-7} pF / \sqrt{Hz}$ down to $\sim 10^{-2}$ Hz corresponding to $\sim 22 \cdot 10^{-12} m / \sqrt{Hz}$.

LISA noise is $\sim 2 \cdot 10^{-9} m / \sqrt{Hz}$ down to $\sim 10^{-4}$ Hz.



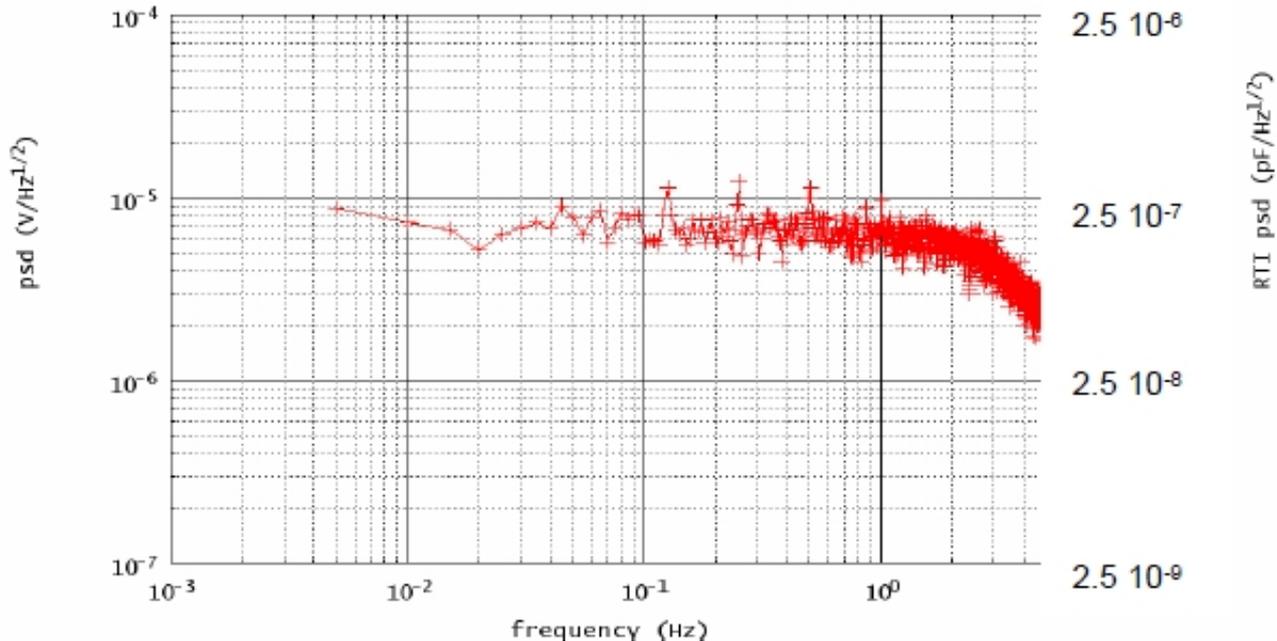
MICROSCOPE bridge noise.

From a recent talk given in Les Houches, October 20—22, 2009
by Manuel Rodrigues. Based on the same ideas as the ONERA bridge.

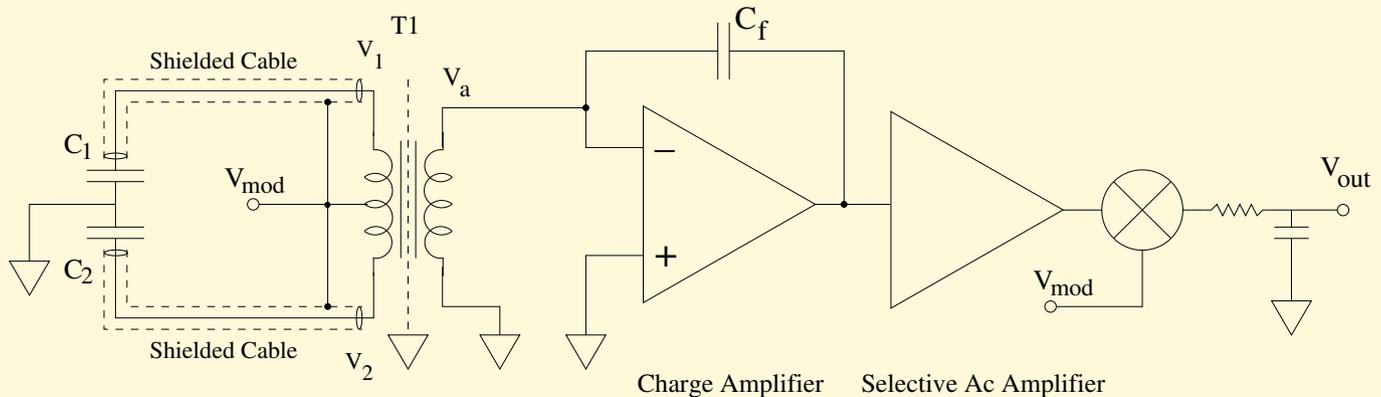
$$\sim 2.5 \cdot 10^{-7} \text{ pF} / \sqrt{\text{Hz}} \text{ down to } \sim 5 \cdot 10^{-3} \text{ Hz.}$$

1 V \sim 0.025 pF \sim 6 μm (with 600 μm elect/mass

gaps) contribution to accelerometer noise: Yli detector
(detector noise referred to input displacement)



Simplified schematics of the new GGG bridge



- We have modified the ONERA circuit.
- The two GGG test masses are connected to the electrical ground.
- The primary of the transformer is connected to the Mod. signal.
- Redesign of the transformer.
- We are now using a commercial lock-in amplifier.

Results of Spice simulation of the new GGG bridge.

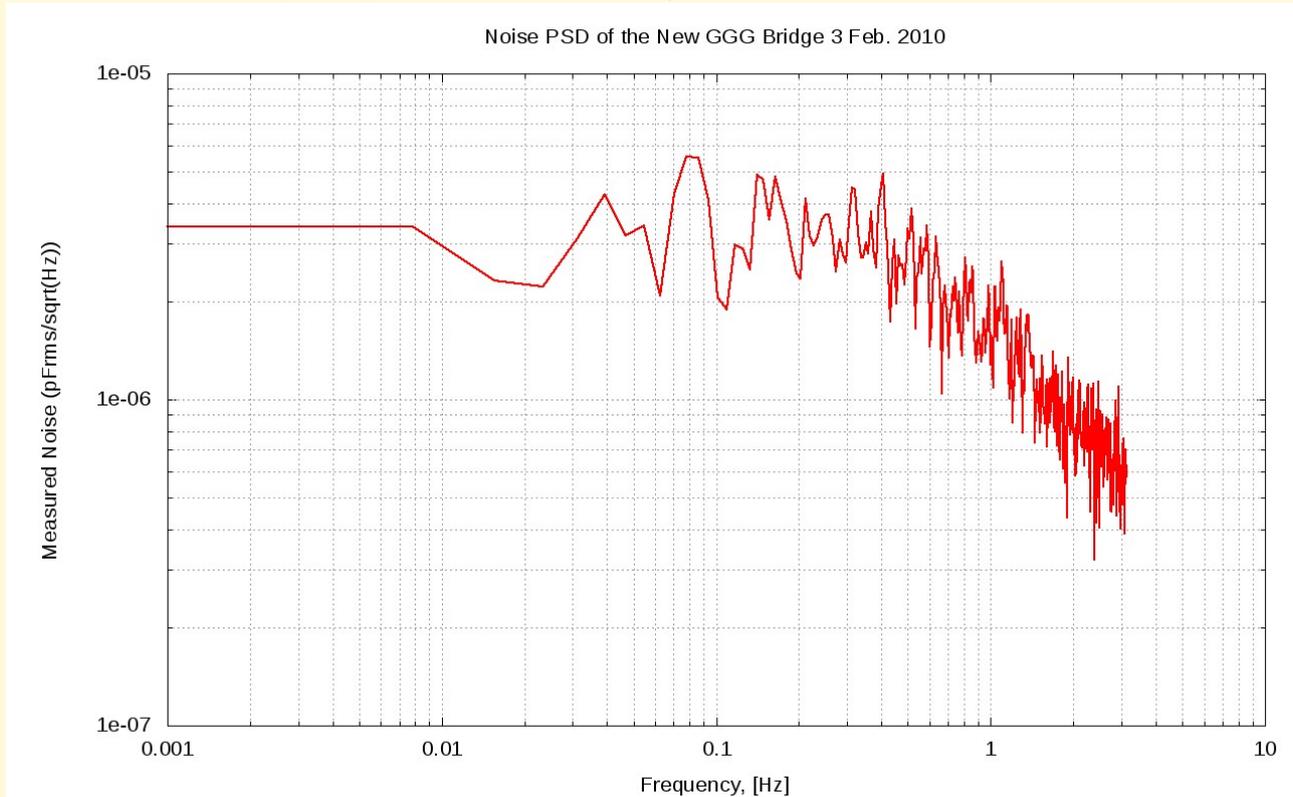
Noise of the modulated signal after the preamplifier.

At the modulation freq. of 100 KHz the simulated noise is $\sim 10^{-7} \text{ pF}/\sqrt{\text{Hz}}$



Measured noise of the new GGG bridge prototype

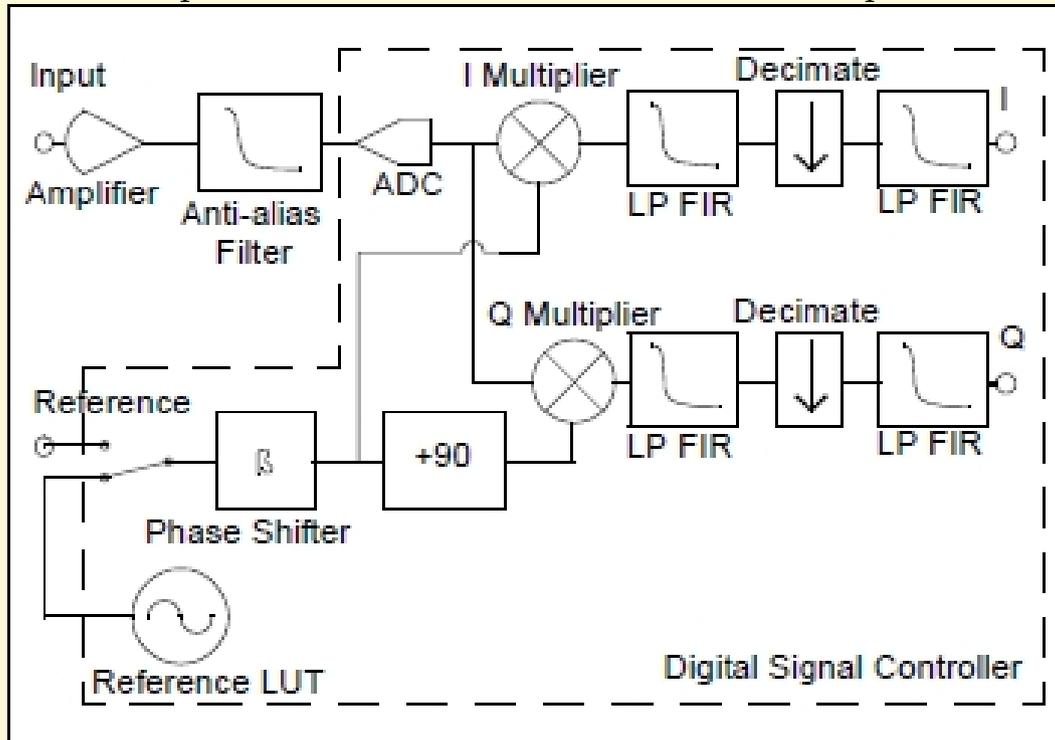
Noise of the demodulated signal. Integration time is 3 sec. that is $f_c \simeq 0.33$ Hz
Obtained a few days ago, $\sim 5 \cdot 10^{-6} pF/\sqrt{Hz}$ at ~ 0.17 Hz, to be improved.



We need a digital lock-in amplifier.

Analog mixers ICs are limited in terms of dynamic range and noise. A digital lock-in amplifier will provide the requested performance. Digitisation of the modulated (≈ 100 KHz) preamplifier signal at 2Ms/sec, 24 bits.

DSP implemented in an FPGA or in a microprocessor.



Present status and Next steps

Present status:

- These are preliminar results.
- Only the “front-end” part of the bridge has been tested, we have used a commercial lock-in amplifier.

Next steps:

- Improve the noise performance and stability of the circuit.
- Design the Digital lock-in amplifier circuit block.